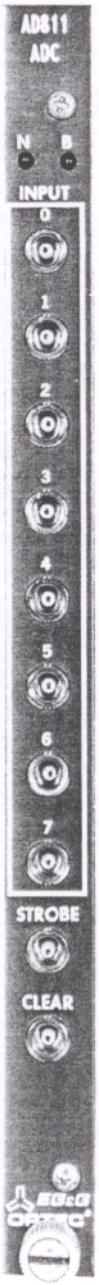
AD811
CAMAC
Analog-to-Digital Converter (continued)

- **Eight peak-measuring ADCs for pulse amplitude spectroscopy**
- **11-bit range (2047 channels) plus overflow**
- **80-μs fixed conversion time**
- **CAMAC readout**
- **Common strobe input**
- **0.5-μs fast clear**
- **Full LAM logic**



The EG&G ORTEC Model AD811 ADC contains eight peak-measuring analog-to-digital converters packaged in a single-width CAMAC module. This unit is designed to measure positive unipolar or bipolar signals from nuclear shaping amplifiers in the range of 0 to +2 V. Because the circuit is completely dc-coupled, this module can be used for sampling dc or slowly changing voltages, thereby allowing a wide range of applications.

The Model AD811 features 1-mV resolution with a range of 11 bits (2047 channels). A 12th bit is included in the data registers for overflow detection. The input linear gates and peak detectors are normally in the closed condition, and the unit must be triggered by an external strobe pulse to start a conversion.

On receipt of a strobe input, an internal gate pulse is generated which opens all eight linear gates and enables the peak detectors. The duration of this gate pulse can be internally adjusted to overlap the peaks of the inputs for correct operation. Alternatively, the width of the external pulse applied to the Strobe input can be adjusted to lengthen the gate pulse beyond the duration set by the internal circuit. At the completion of the sampling period, a Wilkinson conversion process is started which proceeds in parallel for eight sections. The total conversion period lasts for approximately 80 μs, and is independent of the input signal amplitude in any channel. At any time during the 80-μs digitizing period, the conversion can be aborted by application of a signal to the front-panel Clear input; the unit will then be fully restored to its quiescent state within 0.5 μs and be ready to accept another strobe. The Model AD811 features full LAM logic and on completion of a normal conversion generates a LAM for service request. This LAM can be controlled and tested at the module level by CAMAC commands in accordance with recommended practice.

Automatic testing and calibration checking of the module are readily accomplished by issuing CAMAC command F(25). This supplies an internal reference voltage to all eight converters and triggers a conversion that results in a request for service and an overrange in all eight channels. This provides a full check of the analog circuits and digital registers in the unit.

Two front-panel indicators monitor the status of the module. Indicator N shows when the Model AD811 is being addressed, and indicator B shows when it is in the blocked condition. A blocked condition can be generated by either the internal Busy latch or a Dataway inhibit signal.

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Specifications

PERFORMANCE

RANGE 0 to >+2 V peak measuring; 2047 channels plus overflow.

RESOLUTION 1.0 mV referred to input.

CHANNEL WIDTH 1.0 mV per channel, 60% flat-top profile.

INTEGRAL NONLINEARITY ≤±0.05% from 1% to 100% of full scale.

DIFFERENTIAL NONLINEARITY ≤±2% from 5% to 100% of full scale.

CONVERSION TIME Fixed at <80 μs for all channels in parallel.

CROSSTALK A 5-V signal of 50 ns or greater rise time will not affect any adjacent section by more than 1 channel.

TEMPERATURE COEFFICIENT ±0.025%/°C (0 to 50°C).

CONTROLS AND INDICATORS

GATE WIDTH Internal potentiometer controls minimum width of gating signal from nominally 50 ns to 350 ns; gating signal should precede peak of data inputs by at least 80 ns and overlap peak for correct operation.

CALIBRATE 8 internal potentiometers to set calibration (slope) of each ADC.

OFFSET 8 internal potentiometers to set zero level of each ADC.

ENABLE/DISABLE I Internal jumper-selectable Dataway inhibit.

B Indicator lights when unit is in blocked condition.

N Indicator lights when unit is being addressed.

INPUTS

INPUT 0–7
Impedance 1 kΩ; dc-coupled.
Polarity Accepts positive unipolar and bipolar inputs having a positive lobe FWHM >50 ns.
Range 0 to >+2 V, peak measuring.
Protection ±5 V dc, ±100 V transient.

STROBE
Impedance 50 Ω; dc-coupled.
Polarity Accepts NIM fast logic signal of >5 ns duration to start conversion; leading edge must precede peak of data signal by at least 80 ns. Strobe input pulse width sets the gate pulse duration if longer than the internally set gate width.
Protection ±5 V dc.

CLEAR
Impedance 50 Ω; dc-coupled.
Polarity Accepts NIM fast logic signal of >5 ns duration; must occur within 80 μs from trailing edge of strobe signal for correct operation.
Reset Time 0.5 μs to 0.1% of full scale.
Protection ±5 V dc.

OUTPUTS

DATA 11 bits per section on R1–R11.

OVERFLOW 1 bit per section on R12 (latching).

LAM Dataway LAM is set at end of conversion; may be enabled/disabled and status-tested by CAMAC commands.

CAMAC CODES

F(0)·A(0–7) Read selected section.

F(2)·A(0–6) Read selected section.

F(2)·A(7) Read section 7 and clear all sections, Busy and LAM.

F(8)·A(12) Test LAM, Q = LAM.

F(10)·A(12) Clear LAM.

F(11)·A(12) Clear LAM, Busy, and Data registers.

F(24)·A(12) Disable LAM.

F(25)·A(0) Test all sections; generates overrun in all channels.

F(26)·A(12) Enable LAM.

F(27)·A(12) Test Busy, Q = Busy.

Q and X Are returned for all above function codes and subaddresses except F(8)·A(12), F(10)·A(12), and F(27)·A(12), where the Q response is conditional.

C Clears all Data registers, Busy, and LAM status.

Z Clears all Data registers, Busy, and LAM status and disables LAM.

I Inhibits operation of all sections.

ELECTRICAL AND MECHANICAL

DIMENSIONS Standard CAMAC single-width module, 1.70 × 22.15 cm (0.669 × 8.721 in.) front panel per IEEE Std. 583-1975.

CONNECTORS LEMO 00C50.

POWER REQUIRED +6 V, 550 mA; −6 V, 250 mA; +24 V, 95 mA; −24 V, 8 mA.

WEIGHT
Net 0.9 kg (2 lb).
Shipping 2.3 kg (5 lb).

Ordering Information

To order, specify:

Model	Description
AD811	CAMAC Analog-to-Digital Converter